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RESEARCH ARTICLE OPEN ACCESS

DESIGN OF A MULTI-LEVEL INVERTER FOR APPLICATIONS IN DISTRIBUTED GENERATION

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ABSTRACT

At present, the use of electricity generation systems through alternative sources of energy is continuously increasing, due to the increase in global energy demand, and a trend in which CO2 emissions are being reduced. As a result of these trends, the implementation of these energy sources has increased steadily in the last quarter of a century. For the integration of these alternative forms of electricity generation to be adequate, especially in the use of solar energy and wind energy, because it is necessary to condition them, it has become latent the need to implement electronic power devices such as inverters (continuous current - alternating current), which currently seek to have small, medium and high power sources of electricity, which meet the requirements of efficiency, quality and safety established by the Commission Federal de Electrician (CFE). In the present work, the design and the implementation of a DC/AC converter (direct current - alternating current) using a topology for the inverter of cascaded H - bridges with independent DC sources in a multilevel configuration of 11 voltage levels of control. Applying the technique of the Selective Harmonic Elimination modulation, technique that allows it by Fourier series analysis appropriately chooses the switching angles for the elimination of harmonics of the most significant low frequency.

I. INTRODUCTION

At present, the use of electricity generation systems through alternative sources or renewable sources of energy (FRE) increases continuously, due to the increase in world energy demand. With the increase in alternative sources of energy interconnected to the electricity system, it is necessary to use new distributed generation strategies with a significant impact on the reduction of CO2 emissions and other pollutants to the environment, which makes the implementation of the FRE, such as geothermal, hydroelectric, tidal, wind or solar plants [1].

With the increase in alternative sources of energy interconnected to the electricity system, it is necessary to use new distributed generation strategies with a significant impact on the reduction of CO2 emissions and other pollutants to the environment, which makes the implementation of the FRE. In the Mexican electricity sector, a growth of alternative energy sources is projected in distributed generation systems interconnected to the RED [2].

The secretary of energy (SENER), projects an average annual growth of 3.5% for the next 15 years. To place the gross consumption at the end of 2029 at 471.59 TWh, while in 2014 the gross consumption was 280.1 TWh. For interconnection in Mexico, standards are established that contribute to increasing the efficiency of alternative energy systems [3].

New technologies based on multilevel converters have been developed mainly in the field of photovoltaic and wind applications with connection to the grid [4].

In the search for a better quality of electrical energy, different inverters have been developed with multilevel technology with a low percentage of total harmonic distortion (DAT) [5]. Among multilevel inverters, three topologies stand out: floating capacitor, anchored diode and cascade H bridges, which have applications in medium and high power, the development of this research is focused on the cascade H bridges topology using a single power source. DC. The main advantage of this structure is the reduced number of semiconductors and firing control circuits, as well as better quality and voltage efficiency, which makes the cascade H-bridge inverter a perfect candidate for photovoltaic applications [6] .

Different modulation techniques can be applied to control a multilevel inverter, some based on high frequency Pulse Width Modulation (MAP), and others with fundamental switching frequency. But there is one that stands out due to its characteristics is the modulation technique known as selective harmonic elimination (ESA). This modulation approach reduces the number of carriers reducing switching losses, total harmonic distortion (DAT) and thus increases the power quality (CP) [7]. There are different algorithms for the application of the ESA, one of them is the genetic algorithm which allows to minimize the selective harmonics and therefore the DAT, this algorithm allows to determine optimal switching angles to eliminate some lower order harmonics, minimizing the distortion of total harmonics, while maintaining the required fundamental voltage [8]. This technique can be applied to multi-level investors with any number of levels.

II. TOPOLOGIES OF MULTILEVEL INVERTERS

Several multilevel converter topologies have been developed, the most common being the H-bridge cascade converters, the anchored diode converter, and the floating capacitor converter, source [9].

II.1 ANCHORED DIODE MULTI-LEVEL INVERTERS

The anchored diode multilevel inverter (IMDA) is characterized by dividing the continuous supply voltage into a certain amount of levels by means of series connected capacitors, the topology for a three-level IMDA is shown in figure 1.

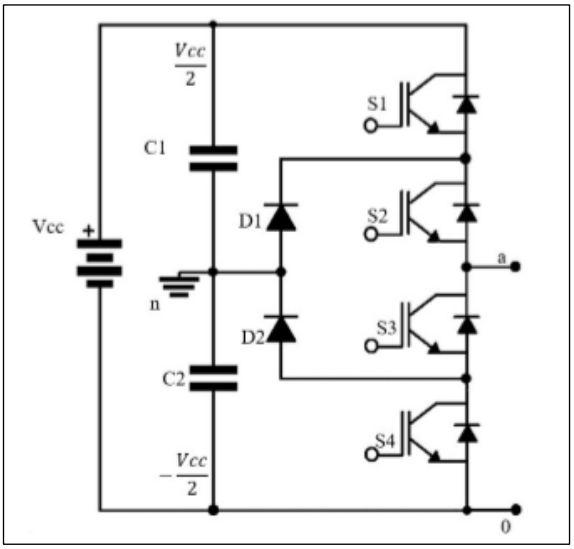

Figure 1: Three Level Anchored Diode Topology.
Source: [9].

In the IMDA topology the number of necessary capacitors is considered (m − 1), in which "m" represents the number of levels of the inverter. In addition, (m − 1) (m − 2) / 2 interlocking diodes are also required, which must be able to block the voltage coming from the capacitor and thus limit the voltage stress of the power devices. As the number of control levels increases, the quality of the output voltage improves and the waveform resembles a sine wave [9].

II.2 MULTILEVEL INVERTERS WITH FLOATING CAPACITORS

The structure of the multilevel floating capacitor (IMCF) inverter is similar to that of IMDA but uses capacitors instead of diodes to set voltage levels. Figure 2 shows the electronic diagram of a three-level single-phase inverter.

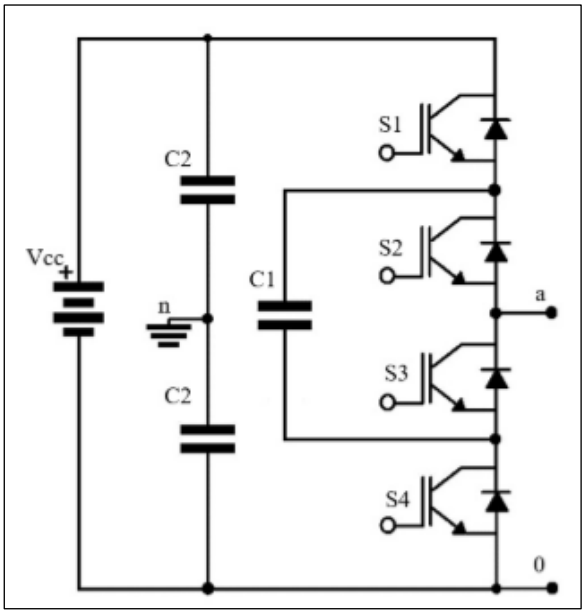

Figure 2: Inverter Topology with Three-Level Floating Capacitors.
Source: [9].

The IMCF of figure 2, for its construction requires (m − 1) capacitors, 2 (m − 1) switches for m desired voltage levels at the output and (m − 1) (m − 2) / 2 auxiliary capacitors per phase. Each capacitor must maintain a fixed voltage; however, because the capacitors are not always charged, the converter has great problems keeping voltage levels balanced. In this case, the modulation technique implemented must correct said problem by implementing a very complex control; furthermore, in this topology it is necessary to previously charge the capacitors before starting to operate as an inverter, therefore, the start-up becomes slow [9].

II.3 MULTILEVEL INVERTERS WITH CASCADE CONNECTED H-BRIDGES

The cascade connected H-bridge multilevel inverter topology (IMPHC) is based on the series connection (or cascade) of several three-level inverters, which are constituted as cells and each of them is powered by a power source independent direct current (DC), which avoids the use of interlocking diodes [9]. Figure 3a shows the topology of a cascade inverter with asymmetric sources and figure 3b shows the waveform for 7 levels.

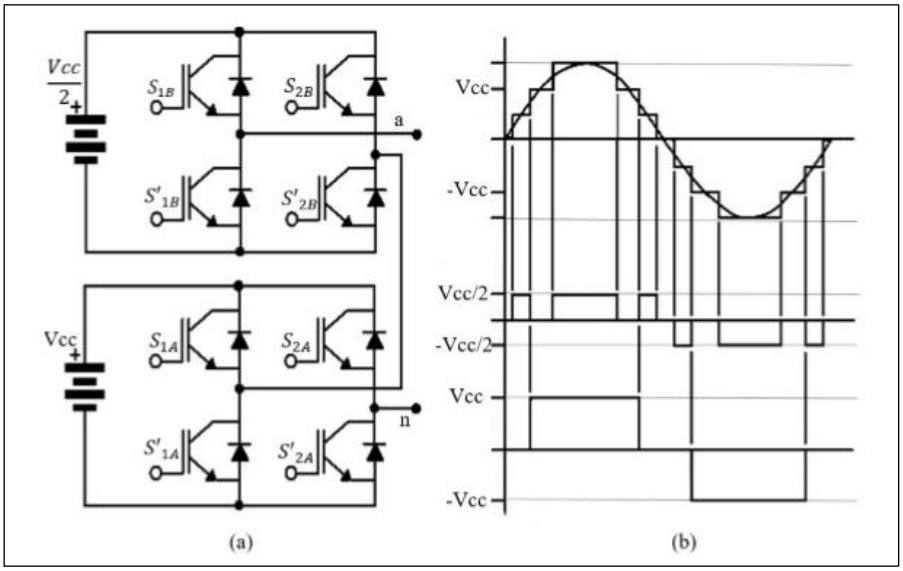

Figure 3: (a) Inverter topology in cascade with asymmetric sources, (b) Waveform for 7 levels.
Source: [9].

As seen in figure 3 (a), the output wave voltage is the sum of the voltages that are generated in each cell, these voltage sums make up a quasi-sinusoidal output wave through different switching arrangements of the semiconductor power devices (DSP), with the option of being controlled by the different existing switching techniques.

Due to its characteristic of having independent DC sources, one of the main advantages of topologies of this type is the possibility of easily increasing the number of levels by adding cells in cascade without having to redesign the power stage. Within the IMPHC, two classifications arise, those that have symmetrical and asymmetric sources, the difference between them lies in the magnitude of the power supply of each inverter. Symmetric inverters require that the power supplies have the same magnitude, while asymmetric ones have voltage sources of different values [9]. This is reflected in the number of levels that can be generated based on the same power-up sequence. Resulting in asymmetric inverters they can generate more voltage levels than symmetric ones.

For an IMPHC of symmetric sources, in this the number of voltage levels at the output is given by m = (2n + 1). Where "m" represents the number of levels, and "n" the number of cells of the inverter. In this inverter the number of voltage levels that can be obtained are 2Vcc, Vcc, 0, -Vcc and -2Vcc. For this type of inverter, in a con figuration with two cells and symmetrical sources, up to five levels can be obtained [9].

In the same way, for a configuration of two cells in cascade, where the second power supply is scaled to twice the first source, there is an IMPHC of asymmetric sources, as can be seen in Figure 3 (a). The generalized waveform for an inverter with 7 voltage levels can be seen in Figure 3 (b), which can be generated from different DSP switching sequences. Table 1 shows the most common sequence used in the literature consulted.

Table 1: Switching sequences for a 7-level IMPHC.

Voltage	S_{1A}	S'_{1A}	S_{2A}	S'_{2A}	S_{1B}	S'_{1B}	S_{2B}	S'_{2B}
1.5 Vcc	1	0	0	1	1	0	0	1
Vcc	1	0	0	1	0	1	1	0
0.5 Vcc	0	1	0	1	1	0	0	1
0	0	1	0	1	0	1	0	1
-0.5 Vcc	0	1	0	1	0	1	1	0
- Vcc	0	1	1	0	1	0	0	1
-1.5 Vcc	0	1	1	0	0	1	1	0

Source: Authors, (2021).

The switching sequence most commonly used in IMPHCs of asymmetric sources to obtain 7 voltage levels is indicated in table 1, where “0” represents that the DSP is off and “1” that the DSP is on.

In the IMPHC of asymmetric sources, up to nine voltage levels can be obtained, a scaling three times greater than the other, this being the maximum number of levels to control as established in equation 1:

$$m = 3^n \quad (1)$$

Where:

“m” represents the number of levels of the inverter, and “n” represents the number of cells of the IMPHC of asymmetric sources.

In the same way, more H bridge cells can be added, each one with its independent DC source and in this way increase the number of levels, being that in an inverter with 3 H bridge cells according to Equation 1 the number of voltage levels will be 27, this configuration being sufficient to meet the objective of this project to degenerate 11 voltage levels.

III. MODULATION TECHNIQUES

The modulation techniques for multilevel algorithms are programs or electronic circuits that manage the DSPs, so that certain levels of the inverter are turned on or off, at the same time they are in charge of regulating the amplitude, frequency and

minimizing the harmonic content of the voltages and Inverter output currents, and depending on the topology, it must be in charge of maintaining the balance of the capacitors in the DC bus.

The main modulation techniques for multilevel inverters are shown in figure 4.

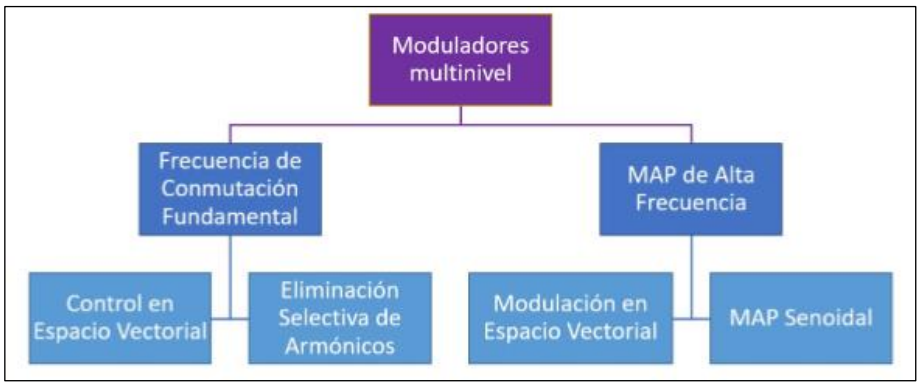

Figure 4: Classification of multilevel modulation methods.
Source: [9].

Figure 4 shows the scheme of the main modulation techniques, which are derived in two main aspects. In the first aspect are those that work at a High Frequency MAP in which there are Modulation in Vector Space and those of multilevel sinusoidal MAP and in the second there are those that work at a Fundamental Switching Frequency, that is, that They work at the frequency of oscillation of the electrical network, within these there are the Control in Vector Space (CEV), and the Selective Elimination of Harmonics (ESA). The importance of modulation techniques is due to the fact that they define the performance of multilevel inverters.

IV. MULTILEVEL INVERTER DESIGN

A prototype of an 11-level multilevel inverter was designed and built using the selective harmonic elimination (SHE) technique, which works autonomously, adjusting to the frequency changes that exist in the electrical grid.

IV.1 MULTILEVEL INVERTER POWER STAGE

The multilevel inverter topology of H bridges connected in cascade with asymmetric sources (IMPHC-FA), is the topology that is best adapted for the development of the multilevel inverter with 11 voltage levels. The IMPHC-FA topology developed for the 11-level inverter design is shown in Figure 5.

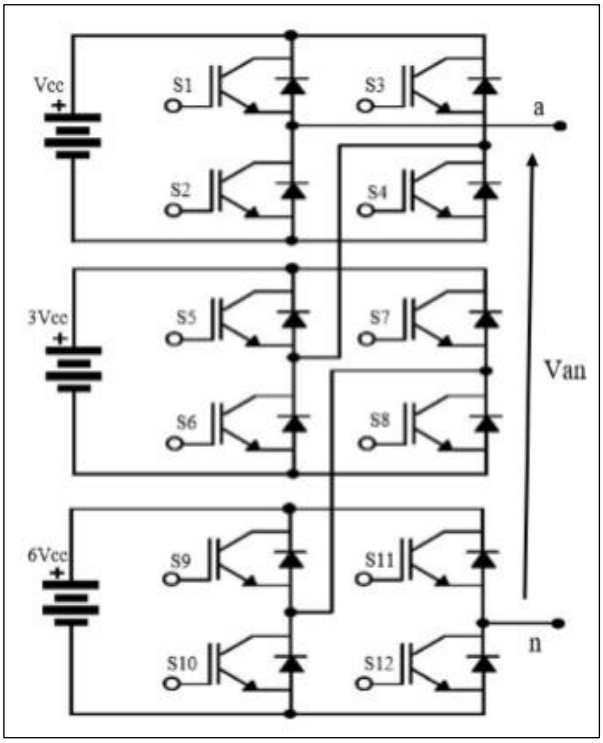

Figure 5: Multilevel inverter with three H-bridges and asymmetric sources.
Source: [9].

From equation 1 it is verified that the proposed topology for the multilevel inverter will be able to provide the 11 voltage levels and thus obtain a quasi-sinusoidal output signal. Digital Signal Processors (DSP) are used to control the IMPHC-FA inverter.

V. MODULATION AND CONTROL STAGE OF THE MULTILEVEL INVERTER

For an adequate selection of DSPs for the control of the IMPHC-FA, it is necessary to know the maximum power, voltages and currents that the power supplies are capable of supplying, which must be independent for each of the H-bridges of the multilevel inverter.

The multilevel inverter developed is powered by a 320W photovoltaic panel, with a maximum voltage and current of 37.4V and 8.56A, which has DC sources designed to operate with the parameters indicated in table 2.

Table 2: Parameters of independent DC sources.

Source	Voltage source (V)	Rated current (A)	Maximum current (A)
Vcc	31.1	0.255	0.856
3 Vcc	93.3	0.755	2.568
6 Vcc	186.6	1.53	5.136

Source: [9].

From table 2 it is observed that the maximum input current is 1.53A, but added to the two smaller bridges, the maximum current for the DSPs is 8.56A, in the same way the blocking voltages have to be considered, which is given by VCC/2. Therefore, an IGBT IRGB4062D transistor was selected as DSP for switching in the multilevel inverter, its main characteristics are shown in table 3.

Table 3: Characteristics IRGB4062D.

V_{CE} (collector emitter voltage)	600V
I_C (collector current)	24A
I_C pulsed (pulsed collector current)	72A
PD (dissipated power)	125W → 200W
Tj (junction temperature)	55◦C → +175◦C
Rθjc (joint thermal resistance)	0.60◦C/W
Rθcd (thermal resistance of sink)	0.50◦C/W

Source: [9].

The selected IGBT IRGB4062D transistor has internally a soft recovery diode in parallel with the transistor which is responsible for protecting the IGBT transistors from reverse currents. Figure 6 shows the power stage for an H-bridge.

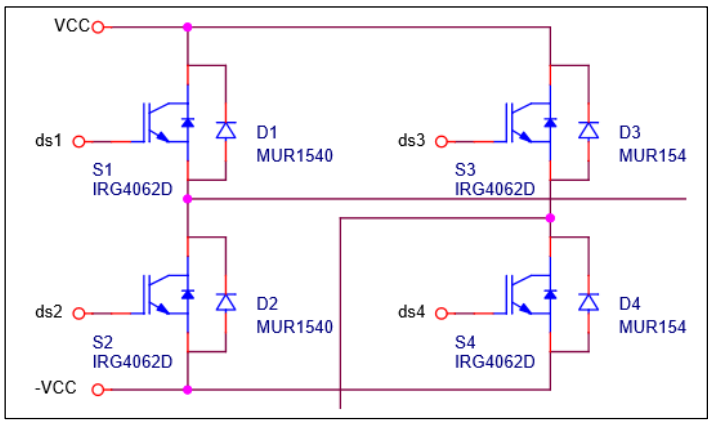

Figure 6: Power stage for an H-bridge.
Source: [9].

The design of the control stage is developed simultaneously with the design of the power stage, given its importance for an adequate switching of the DSPs, as well as to be able to control the voltage and current levels, keeping them at constant levels to allow an adequate interconnection of the multilevel inverter to the electricity grid.

The control strategy used is based on Selective Harmonic Elimination (ESA), which, in addition to maintaining constant voltage and current levels, has the characteristic of being able to selectively eliminate low-frequency harmonics, reducing the percentage of harmonic distortion total (DAT), also only filters are used to eliminate high frequency harmonics.

For the use of the ESA, it is necessary to consider the output waveform of the multilevel inverter, for the above, the generalized waveform for 11 voltage levels is proposed, which can be seen in figure 7.

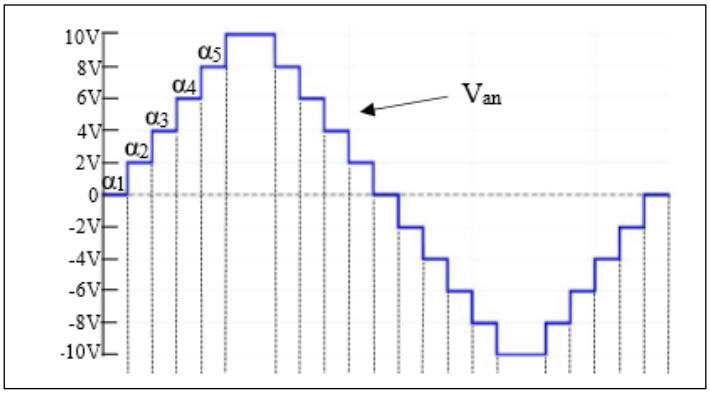

Figure 7: Generalized waveform for an inverter with 11 voltage levels.
Source: [9].

From the generalized waveform of Figure 7, the waveforms that each of the H-bridge cells of the multilevel inverter will have can be determined. Figure 8 shows the waveforms for each H-bridge of the 11-level inverter.

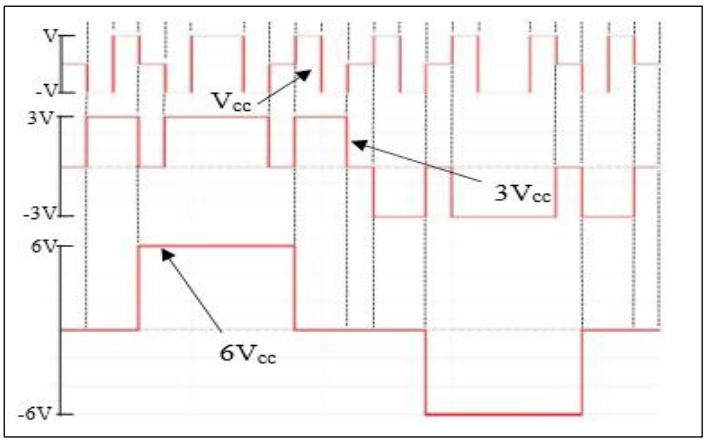

Figure 8: Waveform determined for each H-bridge of the 11-level multilevel inverter.
Source: [9].

Figure 8 shows the output waveform that was determined for each of the H bridge cells, where each one represents the inverter cell with the same name of the desired power supplies for the 11 inverter levels that is Vcc, 3Vcc and 6Vcc.

From the waveforms that were determined in figure 8, it is possible to obtain the switching sequences for each of the IGBT transistors. Table 4 shows the switching sequences for the 11-level multilevel inverter.

Table 4: Switching sequences for the 11-level multilevel inverter.

Volts	S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11	S12
0	0	1	0	1	1	0	1	0	1	0	1	0
2	0	1	1	0	1	0	0	1	1	0	1	0
4	1	0	0	1	1	0	0	1	1	0	1	0
6	1	0	1	0	1	0	1	0	1	0	0	1
8	0	1	1	0	1	0	0	1	1	0	0	1
10	1	0	0	1	1	0	0	1	1	0	0	1
8	0	1	1	0	1	0	0	1	1	0	0	1
6	1	0	1	0	1	0	1	0	1	0	0	1
4	1	0	0	1	1	0	0	1	1	0	1	0
2	0	1	1	0	1	0	0	1	1	0	1	0
0	0	1	0	1	1	0	1	0	1	0	1	0
-2	1	0	0	1	0	1	1	0	1	0	1	0
-4	0	1	1	0	0	1	1	0	1	0	1	0
-6	1	0	1	0	1	0	1	0	0	1	1	0
-8	1	0	0	1	0	1	1	0	0	1	1	0
-10	0	1	1	0	0	1	1	0	0	1	1	0
-8	1	0	0	1	0	1	1	0	0	1	1	0
-6	1	0	1	0	1	0	1	0	0	1	1	0
-4	0	1	1	0	0	1	1	0	1	0	1	0
-2	1	0	0	1	0	1	1	0	1	0	1	0
0	0	1	0	1	1	0	1	0	1	0	1	0

Source: Authors, (2021).

These switching sequences for each of the IGBT transistors, which are observed in table 4, where "1" indicates that the IGBT is on and "0" that it is off, are complemented by the switching or tripping times that They will be obtained through the ESA application, thus allowing them to be obtained at the inverter output.

The control stage was implemented with an ATMEGA 2560 micro-controller, found in Arduino boards which uses the open source programming language, the schematic diagram is shown in figure 9, [10].

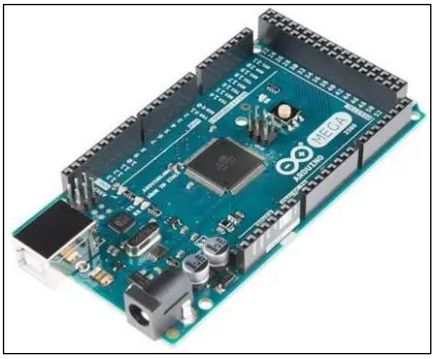

Figure 9: Arduino MEGA 2560.
Source: [10].

Said control stage based on the ATMEGA 2560 micro-controller in Figure 9, focuses on the processing of the switching sequences for the inverter transistors, taking the zero-crossing reference signal from the grid for its start, as well as real-time monitoring of voltage and current signals, which will allow knowing the frequency, power factor and harmonic spectrum values.

The control stage must be completely isolated from the power stage of the multilevel inverter and from the reference signals of the grid, so it is necessary to implement opto-couplers and a conditioning stage for the switching sequences. According to the characteristics of the Arduino MEGA, it can only provide outputs of maximum 5V and 50mA and according to the requirements of the IGBT IRGB4062D transistor it needs an input in its gate of 20V and 200nA.

For the design of the trigger conditioning stage of the IGBT transistors, the 4n26 opto-coupler was selected for the isolation of the control stage and the IR2101 driver for conditioning the trigger signals, which is capable of conditioning voltage and current at constant levels for use in IGBT transistors.

The conditioning circuit for the trigger signals was con fi gured to obtain at the output of the IR2101 driver the 20V output required by the IGBT transistor, this circuit that is observed in Figure 10, that is, opto-coupler, driver, and transistor is useful for half a bridge so it will be necessary to implement 6 similar circuits.

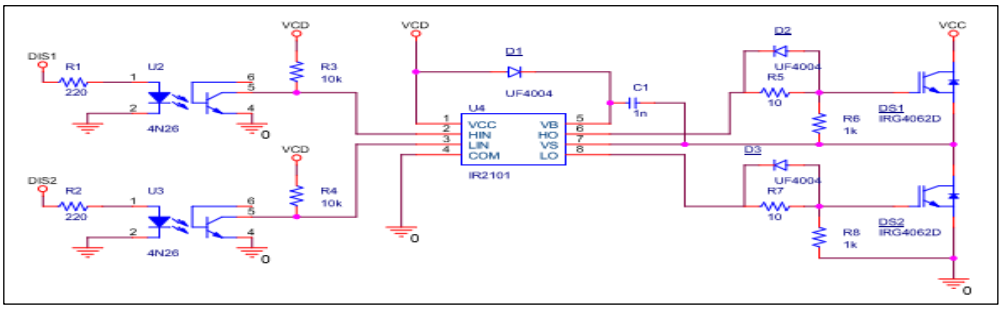

Figure 10: Conditioning circuit for trigger signals.
Source: Authors, (2021).

The switching signals are processed in the micro-controller and directed through the outputs of the digital pins towards the opto-couplers, in order to isolate the control stage, the signal that comes out of the opto-coupler, will be the input of the driver which will be injected into the gate of the IGBT transistor to turn it on and off.

VI. TESTS AND RESULTS

Different tests were carried out on the developed prototype, in the same way the results obtained by means of a commercial network analyzer system (Fluke 43BPowerQualityAnalyzer) are shown, which allows, among other functions, to obtain the values calculated in the prototype.

To carry out the initial tests of the system, a purely resistive load was implemented.

Figure 11 shows the voltage, current and power waveforms obtained by the prototype for a purely resistive load fed by the multilevel inverter and figure 12 shows the voltage and current waveforms for the Fluke 43B system.

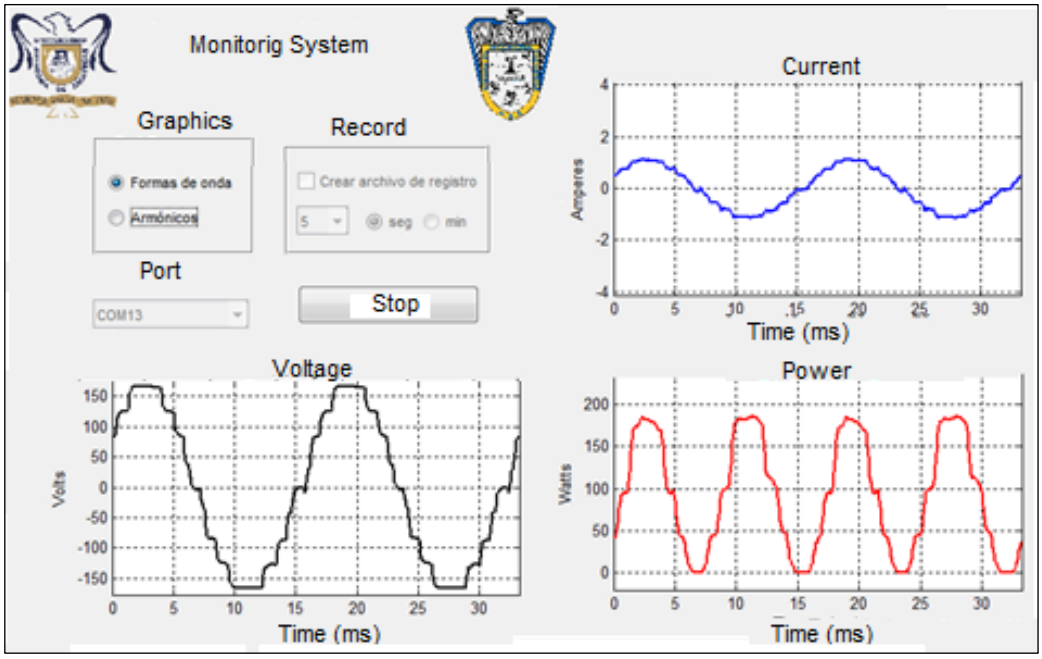

Figure 11: Waveforms obtained in the prototype with the multilevel inverter and resistive load.
Source: Authors, (2021).

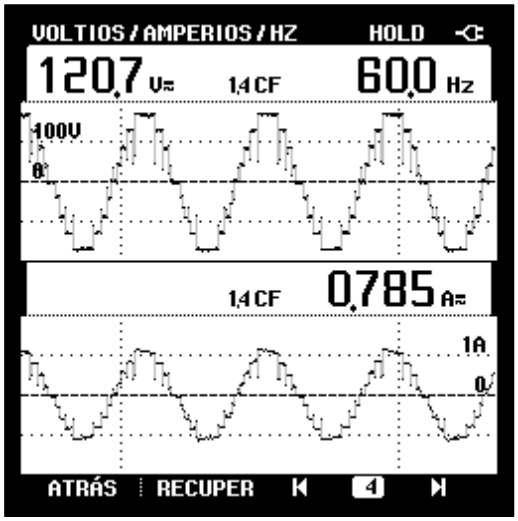

Figure 12: Waveforms Obtained by Fluke 43B Analyzer with Multilevel Inverter and Resistive Load.
Source: Authors, (2021).

Figure 13 shows the graphs of voltage, current and power harmonic components obtained by means of the prototype for a purely resistive load fed by the multilevel inverter, and figure 14 shows the voltage, current and power harmonic components corresponding to the Fluke 43B system.

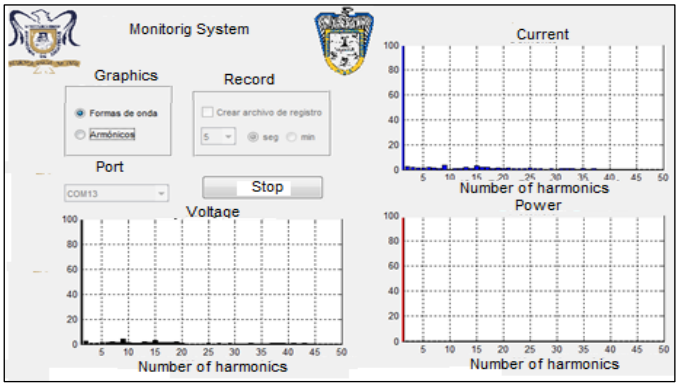

Figure 13: Harmonic components obtained through the prototype with the multilevel inverter and resistive load.
Source: Authors, (2021).

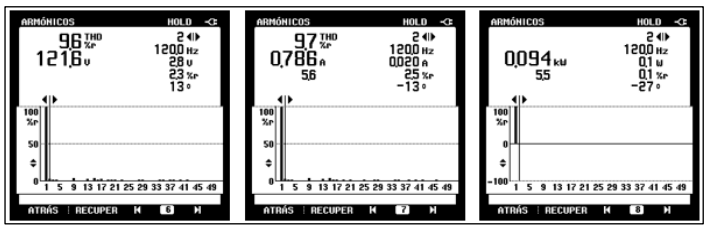

Figure 14: Harmonic components obtained by Fluke 43B analyzer in multilevel inverter with resistive load.
Source: Authors, (2021).

Figure 15 shows the voltage, current and power waveforms obtained by the prototype for a resistive-inductive load fed by the multilevel inverter, and figure 16 shows the voltage and current waveforms for the Fluke 43B system.

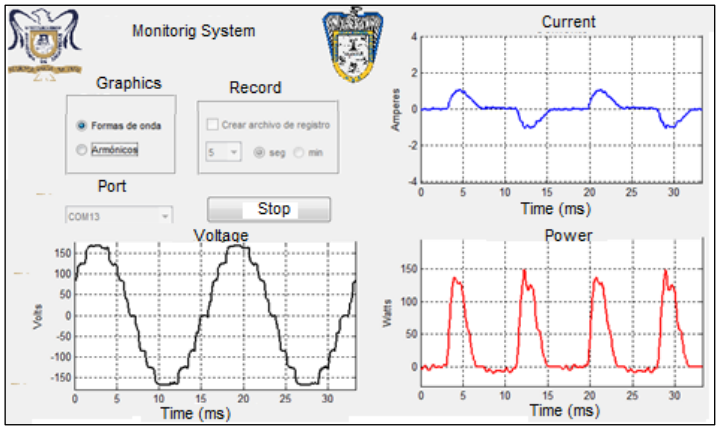

Figure 15: Waveforms obtained with the prototype in the multilevel inverter and inductive-resistive load.
Source: Authors, (2021).

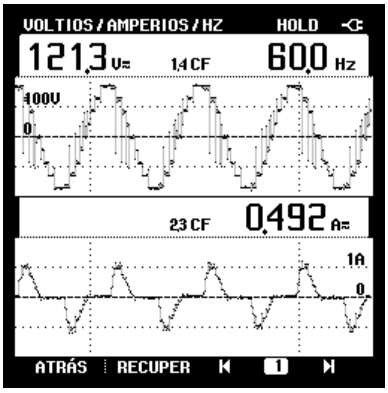

Figure 16: Waveforms Obtained by Fluke 43B Analyzer on Multilevel Inverter with Resistive Inductive Load.
Source: Authors, (2021).

Figure 17 shows the graphs of voltage, current and power harmonic components obtained by means of the prototype for a resistive-inductive load fed by the multilevel inverter, and figure 18 shows the voltage, current and power harmonic components corresponding to the Fluke 43B system.

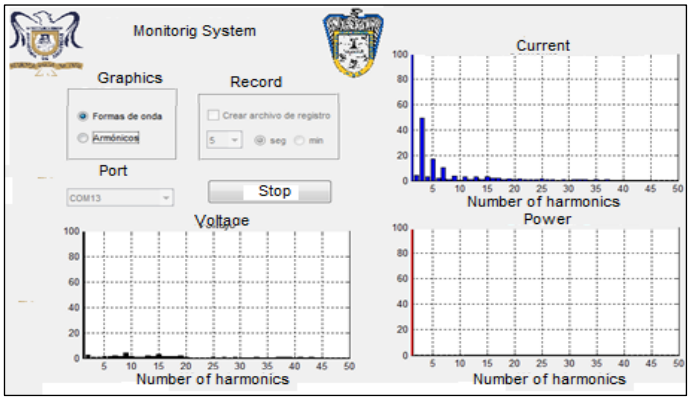

Figure 17: Harmonic components obtained through the prototype in the multilevel inverter with inductive-resistive load.
Source: Authors, (2021).

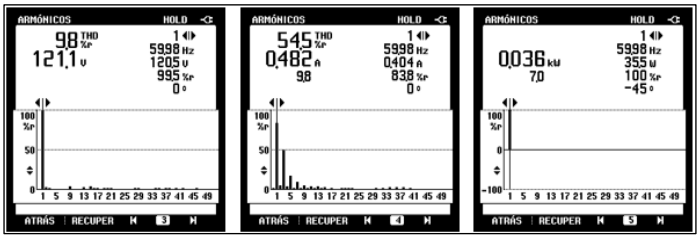

Figure 18: Harmonic components obtained by Fluke 43B analyzer in multilevel inverter with inductive-resistive load.
Source: Authors, (2021).

VII. CONCLUSIONS

Using the methodology developed in this article, the system reproduces the waveforms of voltage, current, power and harmonic components present in the electrical network, in addition, it calculates values of voltage and effective current, active, reactive and apparent power, network frequency and power factor with an acceptable level of precision which allows an accurate record of electrical energy consumption to be carried out.

For the control of the multilevel inverter, the selective harmonic elimination (SHE) technique was used, which is a static modulation technique, so the prototype works autonomously, adjusting to the frequency changes of the electrical NETWORK, which It was synchronized by a transformer.

The prototype shows a low percentage of error compared to the values obtained using commercial systems.

With the magnitudes of voltage, current, power and harmonic components, obtained with the prototype, the quality of electrical energy can be improved, thus avoiding penalties from the electricity company.

VIII. AUTHOR'S CONTRIBUTION

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