Journal of Engineering and Technology for Industrial Applications

ISSN ONLINE: 2447-0228

ITEGAM-JETIA

Manaus, v.7 n.30, p. 37-44. Jul/Aug, 2021

DOI: https://doi.org/10.5935/jetia.v7i30.769

RESEARCH ARTICLE OPEN ACCESS

DESIGN AND ANALYSIS OF QCA ADDER CIRCUITS FOR EFFICIENT COMPUTATION

Jency Rubia J*[1] and Babitha Lincy R[2]

[1] Asst. Prof. Department of ECE, M.A.M College of Engineering and Technology, Tiruchirappalli, India.
[2] Research Scholar, Department of ECE, Sri Venkateswara College of Engineering, Sriperumbudur, India.

[1] http://orcid.org/0000-0002-0088-3611, [2] http://orcid.org/0000-0003-2520-2410

Email: *jencyrubia@gmail.com, rblincy@gmail.com

ARTICLE INFO

Article History
Received: August 07th, 2021
Accepted: August 23th, 2021
Published: August 31th, 2021

Keywords:
QCA (Quantum-dot Cellular Automata),
Quantum Mechanics,
Half adder,
Full adder.

ABSTRACT

QCA technology is considered a viable alternative for CMOS technology since it solves most of the CMOS implications. The Quantum dot Cellular Automata is a computer software program that relates a discrete dynamical system with quantum mechanics. Quantum mechanics is a kind of physics about subatomic particles and which has many interesting properties. The QCA offers very great switching speed and consumes power dissipation extensively. The logic circuits play an essential role in the branch of computer arithmetic. In this paper, the adder circuits have been designed using the novel transistor-free technology called QCA. In addition to that, the planned work has been investigated with CMOS technology. The proposed work is simulated and synthesized by QCA designer suit 2.0.3.

I. INTRODUCTION

Recently, CMOS technology has confronted many physical challenges due to the shrinking gate length in a transistor. To overcome such shortcomings of the conventional CMOS technology, there is a need for effective alternative technology. The ITRS listed some technologies; among them, QCA has many mesmerizing features [1][2]. The scientist Craig S. Lent first proposed this fascinating technique in the year 1993 [3]. QCA is a new computing tool that can signify binary information depends on the spatial sharing of electron charge arrangement in chemical molecules [4]. The computation of cellular automata consists of an array of quantum dots. The Columbic interaction between the QCA cells is only the source of computational power. Otherwise, there is no current movement among cells and no additional outer source of current to the internal cells [5]. Thus, the interconnection between the cells is possible due to the reorganization the electron positions [6]. Since QCA was introduced in 1993, various experimental devices and logic circuits have been developed [7-11]. Though, these devices are not in practical yet, current research evidence that the QCA may eventually attain high density [12], fast switching speed [13], and room heat operation [14].

In this research work, the adder circuit has been designed using QCA technology. The addition is the basic arithmetic operation and is essential in all digital supercomputers and calculators. To enhance the QCA adder cell performance and optimization of the QCA cell, here, Majority Gate (MG) logic structure has been used. There are many types of logic styles for designing circuits in QCA, such as majority gate (MG), and-or-inverter (AOI) and nand-nor-inverter (NNI), logics [15-17]. The subsequent design instructions are considered for the QCA implementation of the proposed adder circuit. The size of the cell is twenty nm by twenty nm. Also, the cell's width and height are assumed to be 18 nm and 5 nm diameter of quantum dots. The cell-to-cell distance is considered as 20 nm between each cell on the grid. These design rules are beneficial to achieve minimum propagation delay due to the cell-to-cell reactions, since there is a limit on the supreme cell amounts in a clock zone. This ensures proper propagation and reliable signal transmission. The proposed QCA adder circuit in this paper has been planned and performed using the QCA designer tool type 2.0.3 with a coherence

simulation engine [18]. The article is prearranged as charts: in section 2, the background of QCA technology and the design approaches are presented. Section 3 describes the design of the adder circuit based on the majority gate logic structure. Chapter 4 shows that the proposed QCA adder and implementation of that. Then section 5 discusses the simulation results, and lastly, the conclusion and future scope are explained in section 6.

II. BACKGROUND OF QCA

II.1 QCA CELL

A QCA cell is a square nanostructure of electron wells restraining free electrons. Every cell contains of four quantum dots that can accommodate a single atom per dot. The four dots are located at the four edges of the QCA cell, and two electrons are infusing into the cell. The two particles are located at the contrary corners of the cell because of the Columbic repulsion principle [19-21]. Thus, this structure provides two conceivable polarizations, as revealed in Figure 1. These elementary QCA cells are beneficial for designing inverter, logic gates, and circuits, memory elements, etc.

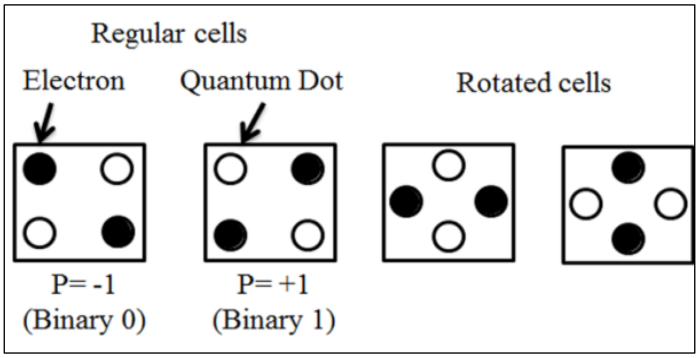

Figure 1: Basic QCA cell and two possible polarizations.
Source: Authors, (2021).

II.2 LOGIC GATES

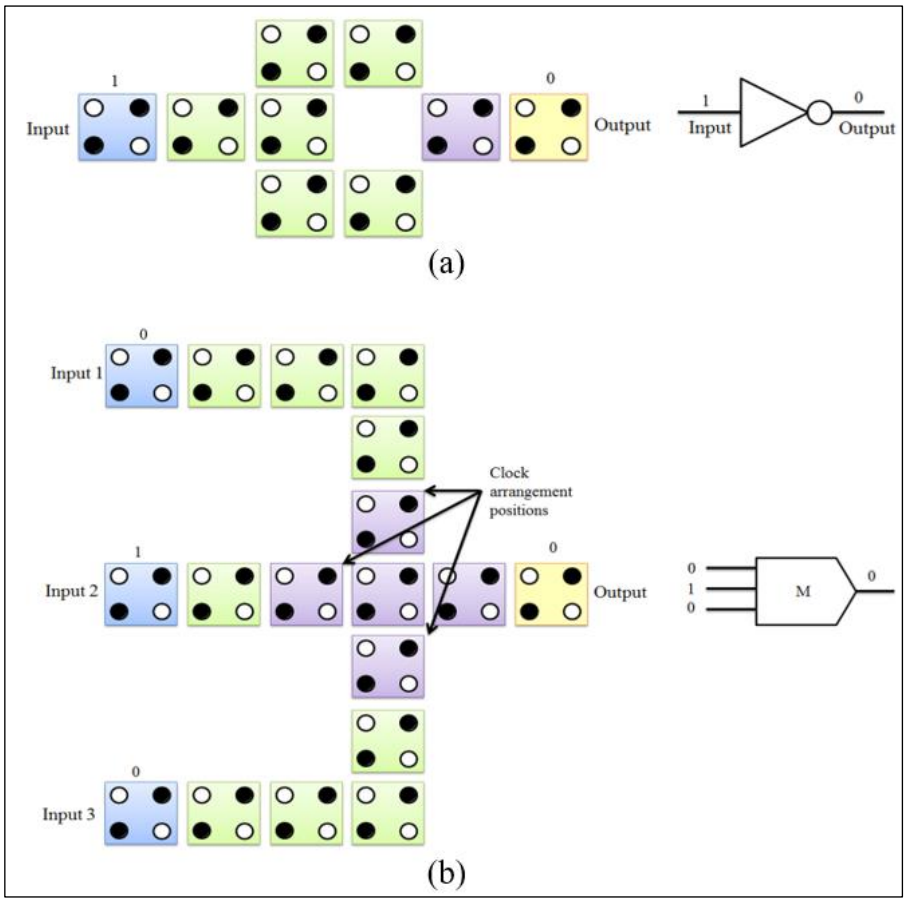

Figure 2: (a) QCA Inverter; (b) Majority gate.
Source: Authors, (2021).

Combination of arithmetic and logical operation. Thus, Logic gates are the elementary building blocks of several arithmetic circuits. In the QCA context, inverters and three-input mainstream gates assisted as an essential gate. Because any logic circuits can be designed using the basic QCA gates. The first equation of the majority gate with inputs a, b, and c in $M(a,b,c) = ab + bc + ca$. Figure 2 illustrates the QCA inverter and the majority gate symbol and layout [22]. Two input AND gate and OR gate can be implemented using the majority gate by making the third input constant. Therefore, utilizing AND, OR, and inverter gates, any logic functions can be achieved. The realization of AND and OR gates are as follows:

$$a.b = M(a,b,0) \quad (1)$$

$$a + b = M(a,b,1) \quad (2)$$

II.3 SIGNAL FLOW AND CONTROL

The consecutive QCA cells are acting like a wire. For a given one clock cycle, the half of the QCA wire is active for signal transmission, but the other half wire is in unpolarized form. During the next clock cycle, the previous active wire portion turned to an inactive state, but the remaining active zone triggers the newly activated cells to be polarized. Like this, signal transfers from one clock zone to another [23]. In general, the circuit area is split into four parts, and four-phase clock signals drive them. Each clock zone consists of four different clock signal stages, such as high-to-low, low, low-to-high, and high. The computation is begun when the clock signal in the high-to-low step and holds the value during the little clock stage. The calculation has also been released when the clock signal at the low-to-high state and inactive during the high state.

III. PROPOSED WORK

III.1 DESIGN OF ADDERS USING MG

Digital computers and other gadgets perform various kinds of arithmetic operations. Among them, addition operation is considered as a most fundamental computation. The proposed work consists of designing adder circuits such as half adder and full adder using the majority gate (MG) logic style [24]. The majority gate plans the suggested work since it reduces the number of gates that required designing an adder circuit. Here, the half adder is designed using four mainstream gates and two inverters, and the full adder is developed directly by using half adders. The full adder's direct design is realized by the QCA addition algorithm, which was proposed by the researcher Walus et al. [25]. This design required two types of wiring of QCA cells. Then the designed adders are implemented with the cell minimization techniques. Hence, the proposed adders consume area and also circuit complexity. The adders are simulated and verified the results according to the truth tables. In the end, the performance analysis of the proposed work has been compared with the common techniques.

III.2 DESIGN OF HALF-ADDER

The half adder is a modest combinational circuit that executes the addition of two bits. The half adder circuit is traditionally designed using EXOR and AND gates. The addition of two numbers A and B processed and the respective outputs are Sum and Carry. From the concept of truth table of the half adder as in Table 1, one can recognize that the Sum output is 1 when either of the inputs (A or B) is 1, and the Carry output is 1 when both the inputs (A and B) are 1. Figure 3 shows the general diagram and Table 1 truth table of the half adder circuit [26].

The logic function of the half adder is,

$$Sum = A'B + AB' \quad (3)$$

$$Carry = AB \quad (4)$$

The QCA representation for the above equation based on MG is,

$$Sum = M\,(M\,(A,B',0),\, M(A',B,0),\, 1) \quad (5)$$

$$Carry = M\,(A,B,0) \quad (6)$$

Figure 3: Schematic diagram of Half-adder.
Source: Authors, (2021).

Table 1: Truth table of the Half-adder.

Inputs		Outputs	
A	**B**	**SUM**	**CARRY**
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Source: Authors, (2021).

III.3 DESIGN OF FULL-ADDER

A full adder is created since there is no facility in a half adder to add carry bits from the lower bits during more than two bits presented in an addition operation [27]. For this purpose only, a full adder circuit has emerged. A full adder is a combinational circuit that achieves the addition of three inputs and produces Sum and Carry as outputs. The block diagram and truth table of the full adder is shown in Figure 4 and Table 2.

Figure 4: Schematic diagram of full-adder.
Source: Authors, (2021).

Table 2: Truth table for full adder.

Inputs			Outputs	
A	**B**	**Cin**	**SUM**	**CARRY**
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Source: Authors, (2021).

III.4 QCA ADDITION ALGORITHM

The design of QCA circuits involves two processes, one is physical design, and another is algorithmic design. For low-level design, it requires any one of the approaches [28]. But, for high-level design, both physical design and algorithmic design needs. Further, more complicated circuit design uses logic design in addition to both the design techniques. Though the QCA circuit design requires physical interactions that are unpleasant and troublesome, the algorithmic design is also a significant aspect of large circuit design. The representation of Carry using Majority Gate logic:

$$\begin{aligned} C_{out} &= AB + BC + AC \\ &= M\,(M\,(B, M(A, C, 1), 0), M(A, C, 0), 1) \\ &= M(A, B, C) \end{aligned}$$

The representation of Sum using Majority Gate logic:

$$\text{Sum} = ABC + A'B'C + A'BC' + AB'C'$$

The plan of full-adder can be implemented in two different approaches. The first technique is direct implementation, a conventional method that requires a lot of area and hardware [29]. The second approach is the Majority gate reduction, this model is simple, and it needs very few hardware requirements. In this work, the majority logic has been used for constructing QCA adders [30, 31]. The planned adders are applied with QCA cells, and the quantity of cells can be reduced by using cell minimization methods. Thus, the implementation further decreases the area and calculation complexity. The direct implementation method of full adder is,

$$\text{Sum} = M(M(A, M(M(B, C, 0), M(B', C', 0), 1, 0), M(A'M(M(B'C, 0), 1), 0), 1) \longrightarrow 11$$

Majority Gates

The implementation of full adder using reduction technique:

$$\begin{aligned}\text{Sum} &= ABC_{in} + A'B'^{C_{in}} + A'BC'_{in} + AB'C'_{in}\\ &= (A.B + A'.B')C_{in} + (A'.B + A.B')C'_{in}\\ &= [A.B + A'.B' + A.C'_{in} + A'.C'_{in} + B.C'_{in} + B'.C'_{in}]C_{in}\\ &\quad + (A'.B + A.B')C'_{in}\\ &= [(A'.B' + A'.C'_{in} + B'.C'_{in}) + (A.B + A.C'_{in} + B.C'_{in})]C_{in}\\ &\quad + (A'.B + A.B')C'_{in}\\ &= [(A'.B' + A'.C'_{in} + B'.C'_{in}) + (A.B + A.C'_{in} + B.C'_{in})]C_{in}\\ &\quad + (A'.C'_{in} + B.C'_{in}) + (A'.C'_{in} + B'.C'_{in})\\ &= [(A'.B' + A'.C'_{in} + B'.C'_{in})C_{in} + (A.B + A.C'_{in}\\ &\quad + B.C'_{in})]C_{in} + (AB + A'.C'_{in}\\ &\quad + B.C'_{in})(A'.C'_{in} + B'.C'_{in} + A'B')\end{aligned}$$

$$\begin{aligned}&= M(A', B', C'_{in}).C_{in} + M(A, B, C'_{in}).C_{in}\\ &\quad + M(A', B', C'_{in})M(A, B, C'_{in})\\ &\quad M[M(A', B', C'_{in}), C_{in}, M(A, B, C'_{in})]\end{aligned}$$

Therefore,

$$\text{Sum=Sum} = M[C'_{out,}C_{in}, M(A, B, C'_{in})] \longrightarrow 3$$

majority gates.

This reduction technique reduces the majority gates from 11 to 3.

IV. QCA IMPLEMENTATION OF ADDERS

The initial step of QCA implementation of adders is designing the adder circuit by the majority gate style. Again, the designed QCA adder circuit has large area and hardware requirements. Thus, cell minimization technique helps to reduce the circuit complexity. Finally, implement the designed adder circuit by QCA cells and compiled by QCA designer.

IV.1 HALF ADDER IMPLEMENTATION

Figure 5 (a) shows that the schematic diagram of the designed QCA half adder requires four common gates and two inverters. The particular QCA implementation of the half adder is illustrated in Figure 5(b). The implementation of half adder is by cell reduction techniques, and it lessens the inverter cells to two, which is designated by the circle in the layout diagram. This proposed work requires implementing the half adder is 77 cells, with a total area of 83160 nm^2, which is much lesser than the existing designs. The previous implementation consists of 105 cells with an area of 108000 nm^2.

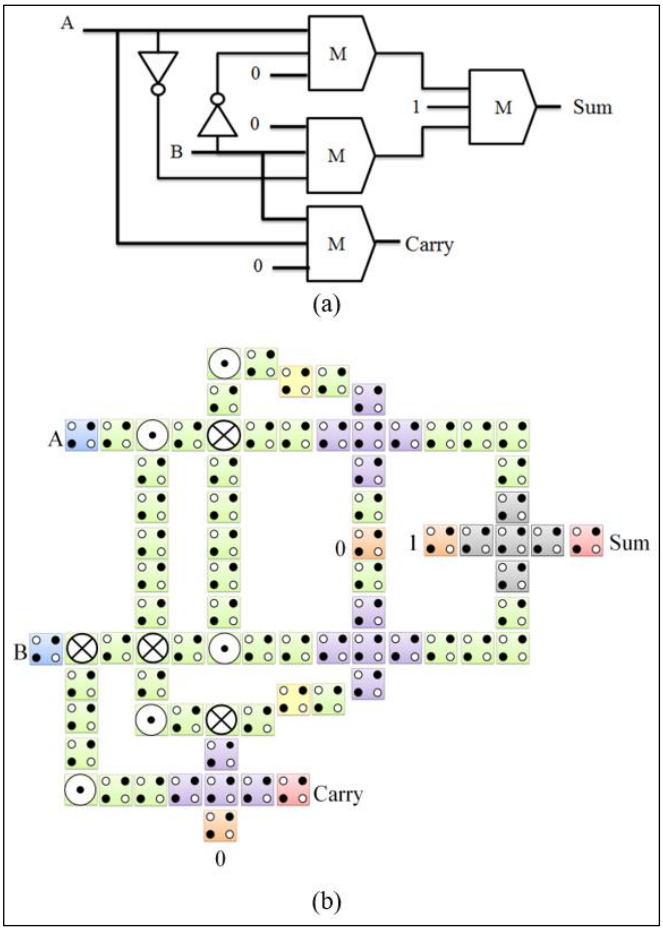

Figure 5: (a) Half adder schematic; (b) Layout of half adder.
Source: Authors, (2021).

IV.2 FULL ADDER IMPLEMENTATION

The full adder can be designed by direct form and by using half adders. The full adder's straightforward implementation is based on the QCA addition algorithm, which was introduced by Zhang et al. [32][33]. The full adder's design using the direct method requires three majority gates and two inverters, as shown in Figure 6(a). Moreover, this type of implementation needs two kinds of wiring methods, such as coplanar and multilayer crossings [34]. These are known as wire crossings. From the two types of crossovers, mainly the coplanar crossover is simple to realize, and it can be used with a slight modification to the basic design. The QCA implementation of a full adder with coplanar crossover is presented in Figure 6(b). The proposed QCA full adder requires 111 QCA cells, and it consumes a total area of 114300 nm^2 which is comparably smaller than the previous implementations. This reduced design is achieved by using two inverter cells and some specific rules for proper cell alignment. The significant QCA design rules are (1) the number of column cells need not be the same, and (2) the minimum distance between the adjacent rows of cells is the width of two cells.

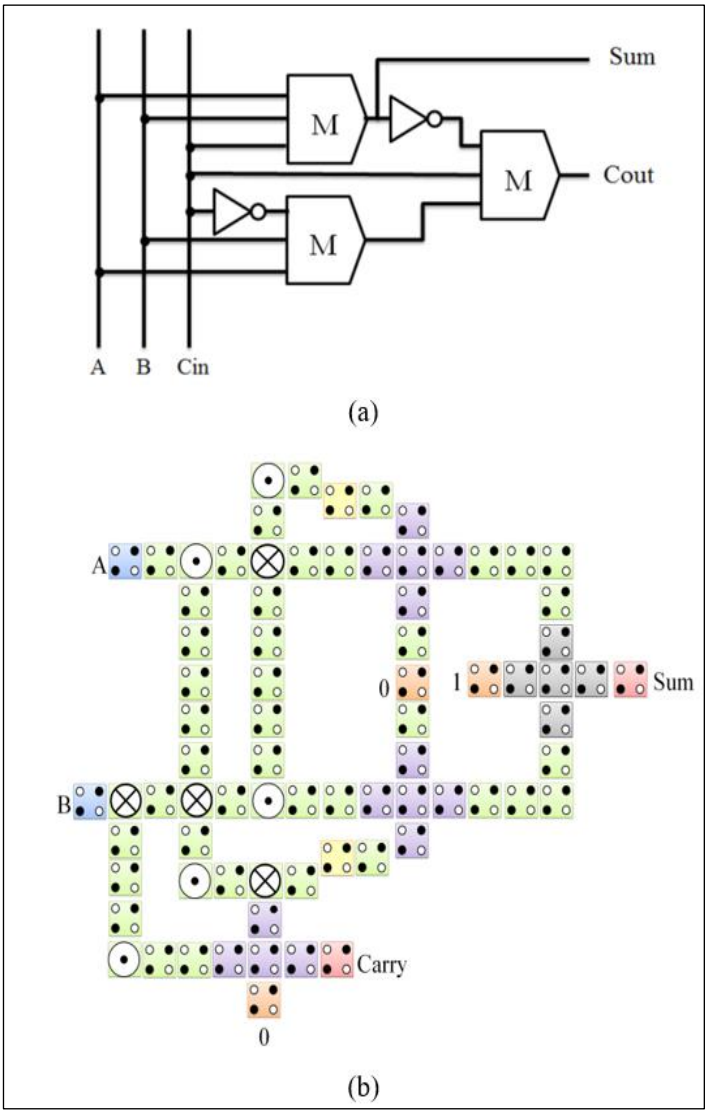

Figure 6: (a) Full adder schematic; (b) Layout of full adder.
Source: Authors, (2021).

Figure 7(a) illustrates the same design of QCA full adder but the position of majority gates and inverters are modified for simple realization. In this method of implementation multilayer crossover has involved which is very straightforward. As the name suggests, it uses more than one layer of cells like a bridge. The equivalent QCA cell implementation is shown in Figure 7(b). This kind of QCA implementation requires 98 cells with a total area of 100800 nm^2 and this also needs less number of cells than the existing implementations.

Another procedure for designing of full adder is using by two half adder circuits and an OR gate. This design consists of 9 majority gates and 4 inverters as presented in Figure 8(a). The respective QCA implementation of the full adder is given in Figure 8(b). Further, this design requires 192 QCA cells, with an area of 208000 nm^2. The Existing implementation needs 218 cells and it consumes an area of 286880 nm^2. At the end, the direct implementation with cell minimization technique provides better performance than this method.

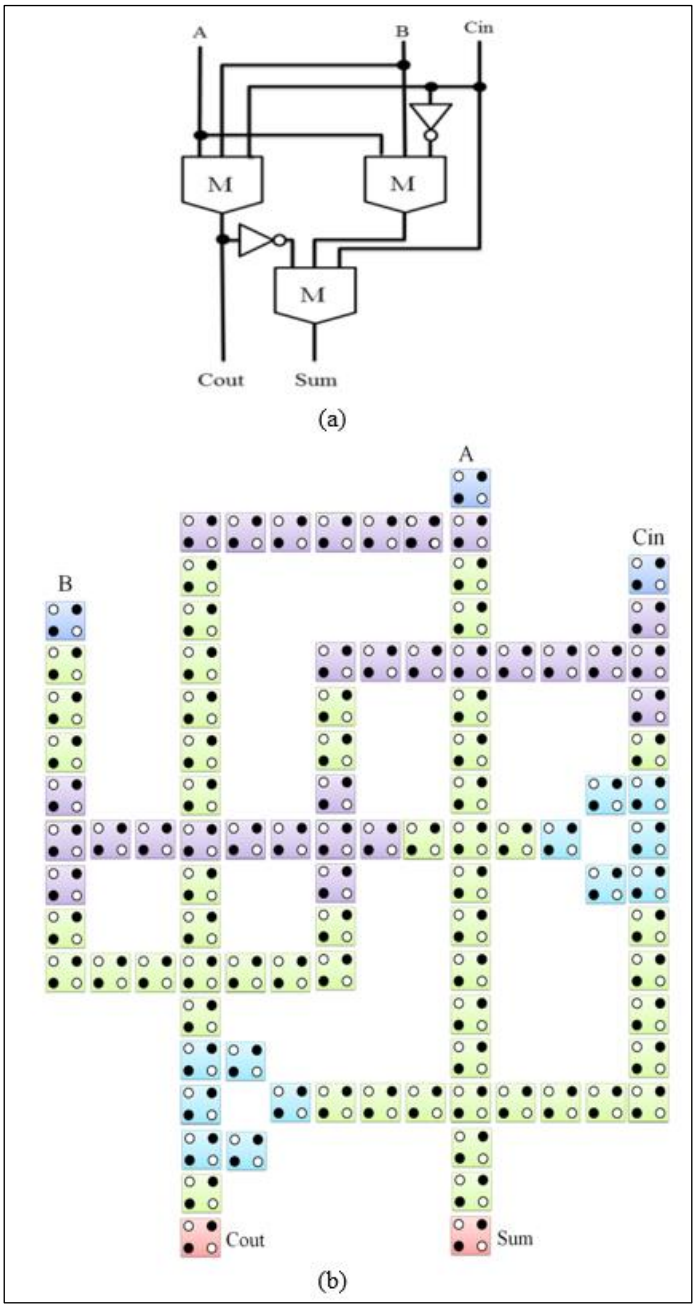

Figure 7: (a) Half adder schematic; (b) Layout of half adder.
Source: Authors, (2021).

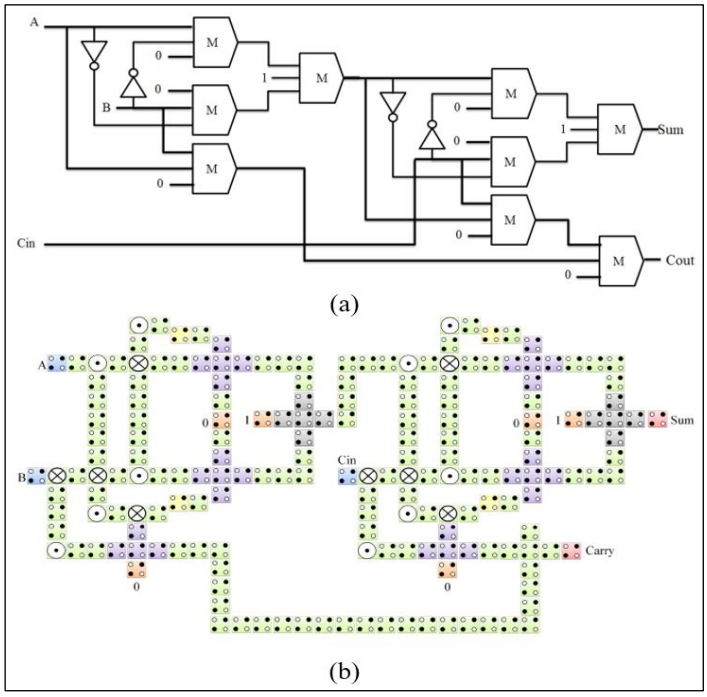

Figure 8: (a) full adder schematic using half adder; (b) Layout of full adder using half adder.
Source: Authors, (2021).

V. SIMULATION RESULTS AND DISCUSSION

V.1 SIMULATION WAVEFORMS

The QCA implementation of half adder and full adder is simulated and synthesized by the QCADesigner 2.0.3 software, and the simulated outputs are shown in 9 and 10. Figure 9 illustrates the QCA simulated waveform of the proposed half adder. The proposed implementation requires four clock phases. Initially, the clock 0 is used to get the inputs, and the clock 1 is used to route the inputs for the majority gate logic. Then, clock 2 is used to process the majority logic gate, and clock 3 used to compute the output. Finally, the output is available in clock 0 again. The sequence of clock 1 to 3 does the following operations, such as setup for hold, relax, and release phase. These phases are used to control the flow of data in the QCA circuits. The same four clock phases are required for operating the QCA full adder and also to produce the output. The simulated results of the QCA full adder are presented in Figure 10.

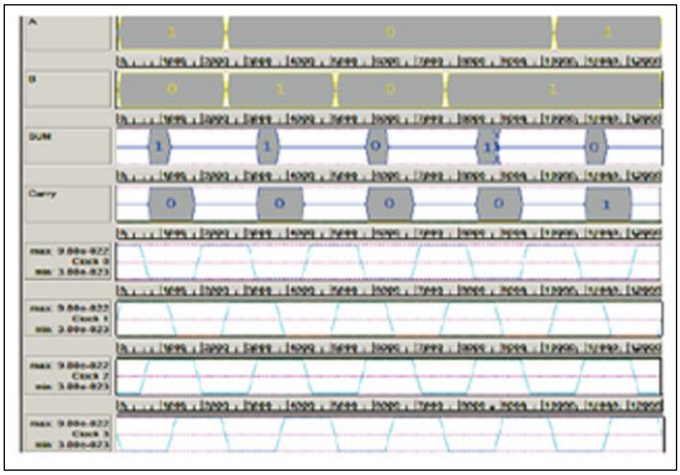

Figure 9: Half adder simulation output.
Source: Authors, (2021).

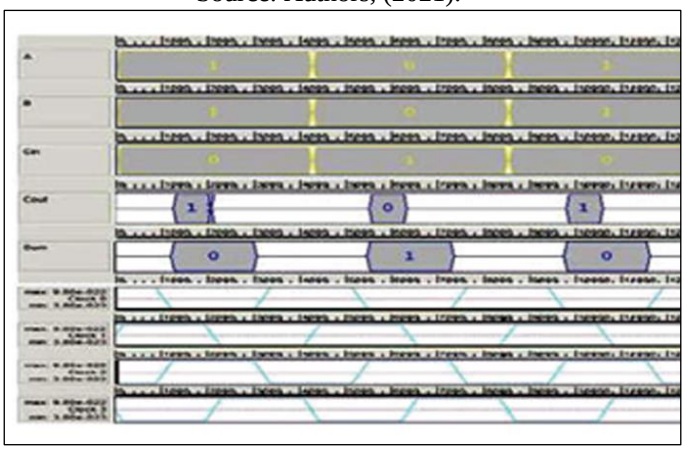

Figure 10: Full adder simulation Output.
Source: Authors, (2021).

V.2 COMPARATIVE ANALYSIS OF QCA ADDERS

The performance analysis of the different types of adders using majority gates is compared with the existing implementations, and CMOS technology is shown in Table 3. The performance analysis of the proposed work compared against factors such as area, complexity, and a number of clock cycles. Moreover, the proposed QCA adders are compared with the previous implementation and existing technology.

Table 3: Comparative performance analysis of proposed technology.

ADDERS		HALF ADDER	FULL ADDER (COPLANAR CROSSOVER)	FULL ADDER (MULTILAYER CROSSOVER)	FULL ADDER USING HALF ADDERS
CMOS	COMPLEXITY	203 CELLS	302 CELLS	-	257 CELLS
	AREA	527 NM×568 NM	652 NM×692 NM	-	450 NM×560NM
PREVIOUS DESIGN	COMPLEXITY	105 CELLS	145 CELLS	137 CELLS	218 CELLS
	AREA	300 NM×360 NM	439 NM×367 NM	435 NM× 300 NM	652 NM ×440 NM
Proposed design	COMPLEXITY	77 CELLS	111 CELLS	98 CELLS	192 CELLS
	AREA	297 NM×280 NM	297 NM×280 NM	360 NM×280 NM	650 NM×320 NM
	NUMBER OF CLOCK CYCLES	1	1	1	2

Source: Authors, (2021).

VI. CONCLUSION

In this paper, half/full adder circuits were designed and analyzed by QCA implementation. The adder circuit is the most basic circuit for any arithmetic computation. By using the Quantum dot-Cellular automata technique, the circuit complexity and area requirement is extensively curtailed. Thereby the performance has been enhanced compared to other technology. The layout and functionality verification has been performed using the software QCADesigner, and the proposed work has compared with the parameters such as complexity, area, and the number of clock cycles. The computation of these adder circuits has been confirmed according to the truth table. From the comparative performance analysis, the proposed layouts are

suggestively smaller than the circuits using CMOS approach. In addition to that, it reduces the required area and complexity for the circuit than the previous QCA circuits. The other arithmetic circuits might be designed using these adder circuits such as subtractors, multipliers, and so on in the future. The designed circuit can be used for image processing, communication, and cryptographic applications.

VI. AUTHOR'S CONTRIBUTION

Conceptualization: Jency Rubia J and Babitha Lincy R.
Methodology: Babitha Lincy R.
Investigation: Jency Rubia J.
Discussion of results: Jency Rubia J and Babitha Lincy R.
Writing – Original Draft: Jency Rubia J and Babitha Lincy R.
Writing – Review and Editing: Jency Rubia J.
Resources: Babitha Lincy R.
Supervision: Jency Rubia J.
Approval of the final text: Jency Rubia J and Babitha Lincy R.

VII. ACKNOWLEDGMENTS

The authors would like to thank the VLSI & DSP laboratory at M.A.M College of Engineering and Technology for providing a suitable environment & facilities, which was very helpful to us in research.

VIII. REFERENCES

[1] Cellular Automata Inverters", International Journal of Computer Applications, Volume 58, No.20, 2012.

[2] C. Lent & P. D. Yougaw, "A Device Archectuure for Computing with Quantum Dots", Proceedings of the IEEE 85, 541, 1997.

[3] Jency Rubia and Bibin Lawrence, "Analysis, Design and Implementation of 4 bit Full Adder Using FinFET", Journal of Convergence Information Technology, vol. 10, no. 2, March 2015, pp. 71-77.

[4] M. A. Peer, K. A. Khan & R. A. Khan "Cellular Automata for Nanoscaled Biological Assemblies", Proceedings of the International Conference on Nanomaterials, NANO, 2005.

[5] Jency Rubia and Babitha Lincy, "Design of Low power 4 bit ALU using 32nm FinFET technology", International Journal Of Pure And Applied Mathematics, vol. 120, no. 6, July 2018, pp. 8089-8099.

[6] C. S. Lent and P. D. Tougaw, "Lines of interacting quantum-dot cells: a binary wire," Journal of Applied Physics, vol. 74, no. 10, pp. 6227–6233, 1993.

[7] M. Askari, M. Taghizadeh, and K. Fardad, "Digital design using quantum-dot cellular automata (a nanotechnologymethod)," in Proceedings of the International Conference on Computer and Communication Engineering (ICCCE '08), pp. 952–955, IEEE, Kuala Lumpur, Malaysia, May 2008.

[8] Jency Rubia and Bibin Lawrence, "Review of Fin FET Technology and Circuit Design Challenges", International Journal of Engineering Research and Applications, vol. 5, no. 12, December 2015, pp. 1-4.

[9] M. Askari, M. Taghizadeh, and K. Fardad, "Design and analysis of a sequential ring counter for QCA implementation," in Proceedings of the International Conference on Computer and Communication Engineering (ICCCE '08), pp. 933–936, May 2008.

[10] A. Orlov et al., "Experimental Demonstration of a Binary Wire for Quantum-Dot Cellular Automata," Applied Physics Letters, vol. 74, no. 19, pp. 2875-2877, May 1999.

[11] J JencyRubia, BG Gopal, V Prabhu, "Ananlysis, Design and implementation of 4 bit full adder using FinFET, Journal of Convergence Information Technolgy, vol 10, Issue 2, PP 71-77.

[12] I. Amlani et al., "Experimental Demonstration of a Leadless Quantum-Dot Cellular Automata Cell," Applied Physics Letters, vol. 77, no. 5, pp. 738-740, July 2000.

[13] Rubia J Jency, Sathish Kumar GA, "A survey paper on modern technologies in fixed-width multiplier," 2017 Fourth International Conference on Signal Processing, Communication and Networking (ICSCN), IEEE Publisher, PP1-6.

[14] R.P. Cowburn and M.E. Welland, "Room Temperature Magnetic Quantum Cellular Automata," Science, vol. 287, no. 5457, pp. 1466- 1468, Feb. 2000.

[15] Rubia JJ, Sathish Kumar G. A high-speed fixed width floating-point multiplier using residue logarithmic number system algorithm. The International Journal of Electrical Engineering & Education. 2020;57(4):361-375. doi:10.1177/0020720918813836

[16] H. Qi et al., "Molecular Quantum Cellular Automata Cells. Electric Field Driven Switching of a Silicon Surface Bound Array of Vertically Oriented Two-Dot Molecular Quantum Cellular Automata," J. Am. Chemical Soc., vol. 125, pp. 15250-15259, 2003.

[17] R.K. Kummamuru et al., "Operation of a Quantum-Dot Cellular Automata (QCA) Shift Register and Analysis of Errors," IEEE Trans. Electron Devices, vol. 50, no. 9, pp. 1906-1913, Sept. 2003.

[18] Rubia JJ, GA SK. Fir filter design using floating point radix 4 algorithm. The International Journal of Electrical Engineering & Education. November 2019. doi:10.1177/0020720919891064

[19] Jency Rubia, Sathish Kumar, "Design and analysis of low power fixed-width multiplier using reduced precision redundancy block," IOSR J. VLSI Sig. Process, Vol 9, Issue 6, pp 1-8.

[20] Kunal Das and Debashis De, "A novel approach of And-Or-Inverter (AOI) gate design for QCA," 2009 4th International Conference on Computers and Devices for Communication (CODEC), Kolkata, 2009, pp. 1-4.

[21] Lee Ai Lim, A. Ghazali, S. C. T. Yan and Chau Chien Fat, "Sequential circuit design using Quantum-dot Cellular Automata (QCA)," 2012 IEEE International Conference on Circuits and Systems (ICCAS), Kuala Lumpur, 2012, pp. 162-167, doi: 10.1109/ICCircuitsAndSystems.2012.6408320.

[22] QCADesigner, Micro Systems and Nanotechnology group (Mina), 2012, http://www.mina.ubc.ca/qcadesigner.

[23] Walus, K., Dysart, T., Jullien, G. and Budiman, R. "QCADesigner: A rapid design and simulation tool for QCA", IEEE Trans. Nanotechnol., Vol. 3, no.1, pp. 26–29, Mar. 2004.

[24] Jency Rubia J, Sathish Kumar G.A, "FIR Filter Design Using Floating point Column Bypassing Technique," International Journal of Recent Technology and Engineering (IJRTE), Volume-8 Issue-2S4, pp 409-413, July 2019

[25] A. DeHon and M.J. Wilson, "Nanowire-Based Sublithographic Programmable Logic Arrays," Proc. Int'l Symp. Field-Programmable Gate Arrays, pp. 123-132, 2004.

[26] Walus, K., Schulhof, G., Jullien, G. A., Zhang, R. and Wang, W. "Circuit design based on majority gates for applications with quantumdot cellular automata," in Conf. Rec. 38th Asilomar Conf. Signals, Systems and Computers, Vol. 2, pp. 1354-1357, 2004.

[27] Wang, W., Walus, K. and Jullien, G. A. "Quantum-dot cellular automata adders", Third IEEE Conference on Nanotechnology, pp. 461-464, 2003.

[28] Afindas A and Naveenkumar S Jency Rubia J, Salim A, " Diagnosis of COVID-19 using ADAM Optimization technique in Convolutional Neural Network (CNN)," Tierärztliche Praxis, Vol 41, pp 415-425

[29] Rubia, J. J., & Sathish Kumar, G. (2020). A high-speed fixed width floating-point multiplier using residue logarithmic number system algorithm. The International Journal of Electrical Engineering & Education, 57(4), 361–375.

[30] Y. Wang and M. Lieberman, "Thermodynamic Behavior of Molecular-Scale Quantum-Dot Cellular Automata (QCA) Wires and Logic Devices," IEEE Trans. Nanotechnology, vol. 3, no. 3, pp. 368-376, Sept. 2004.

[31] A. Bharti and A. Sharma, "Implementation of Ex-OR gate using QCA with NNI logic," 2017 International Conference on Wireless Communications, Signal

Processing and Networking (WiSPNET), Chennai, 2017, pp. 2027-2031, doi: 10.1109/WiSPNET.2017.8300117.

[32] J.M. Seminario et al., “A Molecular Device Operating at Terahertz Frequencies: Theoretical Simulations,” IEEE Trans. Nanotechnology, vol. 3, no. 1, pp. 215-218, Mar. 2004.

[33] Jancy RUBIA J, Babitha Lincy r, Al-Heety, "Moving vehicle detection from video sequences for Traffic Surveillance System," ITEGAM-JETIA, Vol 7, Issue 27, PP 41-48

[34] Jency Rubia J., Babitha Lincy R. (2021) Digital Image Restoration Using Modified Richardson-Lucy Deconvolution Algorithm. In: Chen JZ., Tavares J., Shakya S., Iliyasu A. (eds) Image Processing and Capsule Networks. ICIPCN 2020. Advances in Intelligent Systems and Computing, vol 1200. Springer, Cham.